

IBM POUGHKEEPSIE

Diagnostic Engineering Publication

1410/7010

Dept. B59, Bldg. 965
Date 11/15/63

Subject: Diagnostic Program CC01A - 1410/7010 Limited CPU
Sequence Number 001 Instruction Test
Replaces New Program

This Program uses no System or Channel Control Cards

This Program should be run only from tape.

Enclosures: 44 Pages
Card Deck for CARD ONLY SYSTEMS (as punched by UP51)
8 Cards - Card Loader (1-7) and 1 Core Clear
160 Cards No. 001-160 Data Cards
1 Card Execute Card

Distribution: 1410
 7010
 Other

CC01A
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CC01A

11/15/1963

1410/7010 LIMITED CPU INSTRUCTION TEST

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2.xx.00.0 TEST DESCRIPTION

2.xx.00.1 MODIFICATIONS

CC01A is the first release version of this program and it does not obselete any program.

2.xx.00.2 DESCRIPTION

CC01 was taken directly from C021 to test enough of the basic instruction set to read in and operate the Tape Control Program. It does not contain any Error Typeouts, Loops, Tad Controls or Options to repeat, it is strictly a special purpose test that runs prior to the Tape Control Program and halts for any error.

The Load Program utilizes a few instructions to Load CC01 and they are: BCE, MRCW, MLCS, BA1, RT, BEX1 , MLCWA and a Branch instruction.

This test will only be used in conjunction with the Tape Control Program operating from tape.

2.xx.00.3 EQUIPMENT REQUIRED

Minimum Storage
One tape Unit on any channel
Console Printer

2.xx.00.4 CARD DECK

7	Cards	L1 Loader
1	Card	Core Clear
160	Cards	Program Cards
1	Card	Execute (Branch to 1972) to operate TC50

2.xx.00.5 ENGINEERING LEVEL

CC01 will operate on any 1410/7010 system unless an Engineering Change modifies the operations of the standard Instruction set.

2.xx.01.0 LOADING PROCEDURES

2.xx.01.1 1410 TAPE INPUT

A. Display and Alter Locations 00000-00011 as follows:

1. $RL^vB000011\$$. If tape unit on E channel
2. $XL^vB000011\$$. If tape unit on F channel

B. Set Mode switch to RUN, Computer Reset and Start.

2.xx.01.2 7010 TAPE INPUT

A. If tape unit is on E channel, use 7010 Load Key and disregard steps (B) and (C)

B. If tape unit is not on E channel, Display and Alter Locations 00000-00011 as follows:

1. $XL^vB000011\$$. If tape unit on F channel
2. $3L^vB000011\$$. If tape unit on G channel
3. $1L^vB000011\$$. If tape unit on H channel

C. Set MODE switch to Run, Computer Reset and Start.

2.xx.02.0 OPERATING PROCEDURES

No special instructions are necessary to run this program. The test is ONE, QUICK check of a portion of the basic instruction set and unless there is an error it immediately reads in TC50 and begins to operate TC50

2.xx.03.0 OPERATING HINTS AND COMMENTS

If there is an error the program will stop. The CE must then consult the listing to find out which instruction failed and determine if he can continue. It is possible to continue to the next instruction by pushing the Start Key. If a number of errors occur it would not be possible for TC50 to operate. If there are a few errors it may be possible that TC50 will work and be able to bring into Core C020 or C021 to completely check out CPU instructions and give the CE the benefit of different Loops and Options.

At Location 01000-01100 is a pattern of characters to be looked at only by the C.E to determine if there are any Information Transfer errors between TAU and CPU.

2. xx. 04. 0 PROGRAM STOPS

 All stops are Error Stops

2. xx. 05. 0 TYPEOUTS

2. xx. 05. 1 NORMAL

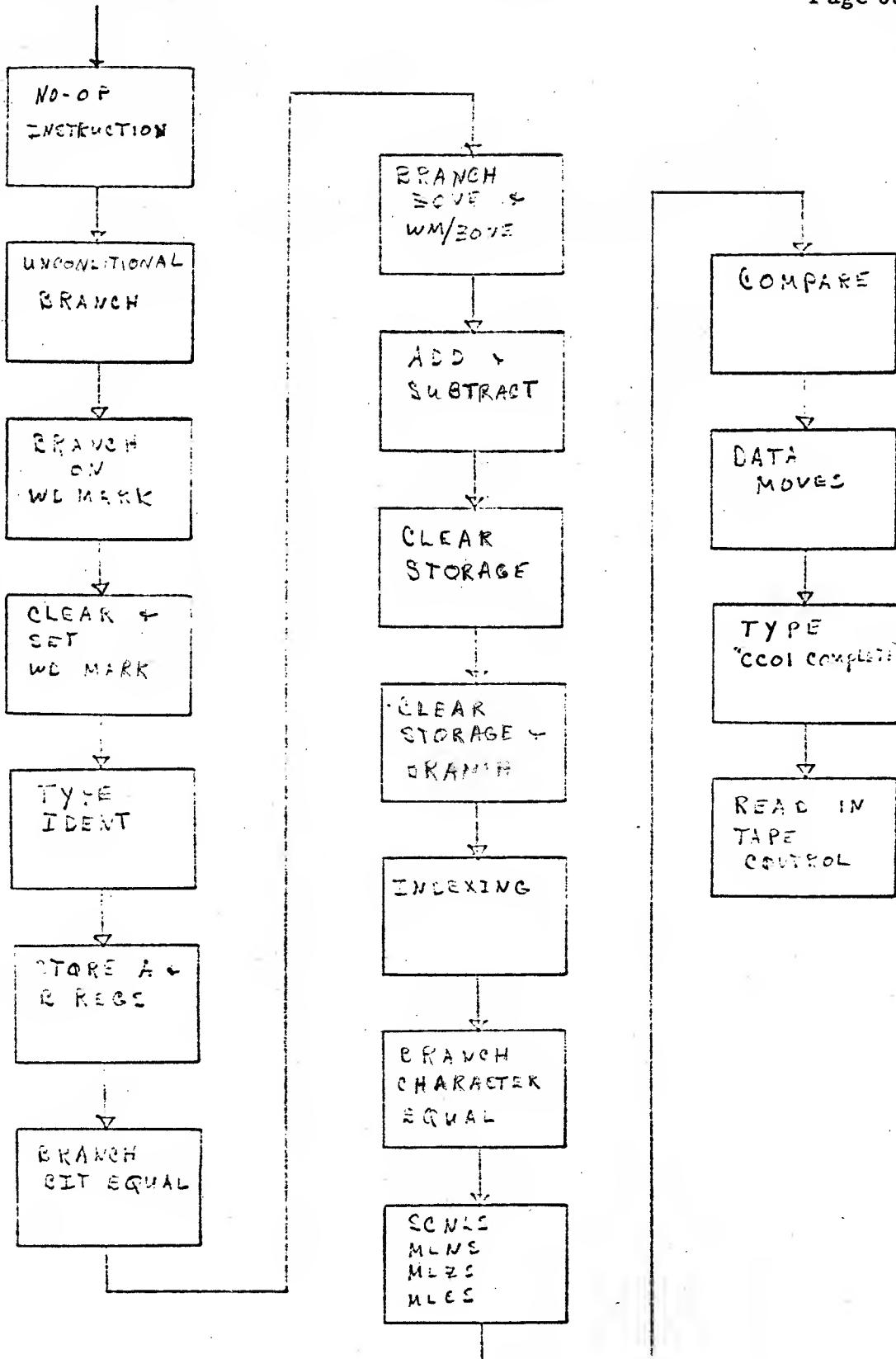
 "CC01A" Test Ident.
 "CC01 COMPLETE" Indicate End of Test.

2. xx. 05. 2 ERROR

 None.

FLOW CHART

CC01
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PGLIN	LABEL	CPU TEST OPCOD	OPERAND	CT	ADDRS	INSTRUCTION	CC01	PAGE	1
10C2		CTL	2						
10C3		LOAD							
1004	CTLIND	EQU	1245						
1005	IDENT	EQU	1250						
1006	START	EQU	2000						
10C7	*								
10C8		DRG	CTLIND				01245		
1009		DC	@0010R3				5	01249	
1010	*								
1011	*	DRG	IDENT						
1012	*	DCW	ACCOLAA.G				5	01254	
1013	*	DRG	1000						
1014	*						01000		
1015	*								
1016	*								
1017		DCW	311223344556677889900AABCCDDEFFFGG2				34	01033	
1018			^HHIIJJKKLLMMNNDOPPPQQRSSTTUUVVWWXX^				34	01067	
1019			^YYZZ .#BTMGS.B,L-/,%SSM#M@.IMM a.G				32	01099	
1020	*								
1021		ORG	1800				01800		
1022	*								
1023		SBR	*E9				7	01800	6 01815 B
1024		WCP	0				10	01807	M ZTO 00000 W
1025		SBR	*E20				7	01817	G 01843 B
1026		BCB1	*-23				7	01824	R 01807 2
1027		BA1	*E1				7	01831	R 01838 G
1028		B	0				7	01838	J 00000
1029	*								
1030	*								
1031		SBR	*E61				7	01845	G 01912 B
1032		RCP	*E26				10	01852	M ZTO 01887 R
1033		BEX1	*-16,M				7	01862	R 01852 M
1034		BNT1	*E32				7	01869	R 01907 S
1035		BA1	*E1				7	01876	R 01883 G
1036		RCPW	0				10	01883	L ZTO 00000 R

INTERNAL ADDRESS ALTER ROUTINE

PGIN	LABEL	CPU TEST	CC01	CC01	INSTRUCTION
		OPCODE	OPCODE	CT	ADDRS
1037	BEX1	*-16, S	7	01893	R 01883 S
1038	BA1	*61	7	01900	R 01907 G
1039	B	0	7	01907	J 00000
1040	ORG	START			
1041		PROGRAM BEGINS HERE			
1042		*****			
1043	*	ROUTINE 01.00 CHECK LONG NC-OP INSTRUCTION			
1044	*	*****			
1045	*	*****			
1046	NOP		1	02000	N
1047	DC	6 1234567890# a GTS / STUVWXYZ+ .XSSM a WBS	32	02032	
1048		2-JKLMN0PQR .S R 0 Q LLG a	32	02064	
1049		2-EABCDEFHIM .D8IM a	*****		
1050	*	*****			
1051	*	ROUTINE 02.00 CHECK UNCOND BR INST. THIS ROUTINE ASSUMES THAT			
1052	*	WM-HL WILL GIVE INSTRUCTION CK IF BRANCH FAILS			
1053	*	*****			
1054	B	*81	SET AND STEP IAR TO SAME ADDRESS	7	02065 J 02072
1055	S	*62	SHOULD SKIP FOLWNG INVALID OPCODE	7	02072 J 02080
1056	DCW	2 2		1	02079
1057	*	*****			
1058	*	*****			
1059	*	ROUTINE 03.00 CHECK BRANCH ON WORD MARK INSTRUCTION			
1060	AC	BW AD,AD	SHOULD NOT BR. INST CK IF IT DOES	12	02080 V 02105 02105 1
1061		BW AE,*61	SHOULD BRANCH. INST CK IF NO BR	12	02092 V 02106 02104 1
1062		DCW 2 2		1	02104
1063	AD	DC 2 2		1	02105
1064	*	*****			
1065	*	ROUTINE 04.00 CHECK CLEAR AND SET WORD MARK INSTRUCTIONS			
1066	*	*****			
1067	*	*****			
1068	AE	CW AC,AE	TRY TO CLEAR WMS AT TWO PLACES	11	02106 H 02080 02106
1069		BW AF-1,AC	SHOULD NOT BR. INST CK IF IT DOES	12	02117 V 02165 02080 1
1070		BW AF,AE	OTTO	12	02129 V 02166 02106 1
1071		SW AE,AC	RESTORE WMS PREVIOUSLY CLEARED	11	02141 * 02106 02080
1072		BW *64,AE	TEST AE FOR WORD MARK	12	02152 V 02167 02106 1

PGIN	LABEL	CC01	CPU TEST	CC01	PAGE
		OPCODE	OPERAND	ADDRS	INSTRUCTION
1073	AF	DCW	a 12@	3	02166
1074		BW	*E2,AC	12	02167 V 02180 02080 1
1075		DCW	a @	1	02179
1076			*****		
1077	*	ROUTINE 05.00	TYPE IDENT, CK TYPEWR BUSY, HALT, HALT/BR.		
1078	*	ROUTINE 05.00	TYPE IDENT, CK TYPEWR BUSY, HALT, HALT/BR.		
1079	*		THESE OPS PERFORMED ONLY FIRST TIME THROUGH		
1080	*		*****		
1081		NOPWM		1	02180 N
1082		B	AJ	7	02181 J 02226
1083		SW	*-12	6	02188 * 02181
1084	AG	WCP	IDENT	10	02194 M ZTO 01250 W
1085		BCB1	*-16	7	02204 R 02194 2
1086		RA1	*E1	7	02211 R 02218 G
1087		ORG	*		
1088	AH	NOP		1	02218 N
1089		B	AJ	7	02219 J 02226
1090		ORG	*		
1091			*****		
1092	*	ROUTINE 06.00	CHECK OPERATION OF SAR AND SBR INSTRUCTIONS		
1093	*	ROUTINE 06.00	CHECK OPERATION OF SAR AND SBR INSTRUCTIONS		
1094	*		*****		
1095	AJ	B	AK	7	02226 J 02233
1096	AK	NOPWM		1	02233 N
1097		B	AL	7	02234 J 02286
1098		SW	AKE1	6	02241 * 02234
1099		CW	1.ANE1	11	02247 □ 00001 02288
1100		SBR	AJ65	7	02258 G 02231 B
1101		SAR	AJ65	7	02265 G 02231 A
1102		SBR	AJ65	7	02272 G 02231 B
1103		R	AJ	7	02279 J 02226
1104	AL	H		1	02286 *
1105	AN	CW	A0E1,2	11	02287 □ 02327 00002
1106		SAR	AJ65	7	02298 G 02231 A
1107		SBR	AJ65	7	02305 G 02231 B
1108		SAR	AJ65	7	02312 G 02231 A

CC01 INSTRUCTION

CPU TEST
OPCODE OPERAND

PGLIN	LABEL	OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
1109		B	AJ	7	02319	J 02226
1110	AO	CW	AK61	6	02326	□ 02234
1111		SAR	AJ65	7	02332	G 02231 A
1112		SH	1	6	02339	, 00001
1113	*****	*****	*****			
1114	*	ROUTINE 07.00	CHECK OPERATION OF BRANCH BIT EQUAL INSTRUCTION			
1115	*	ROUTINE 07.00	CHECK OPERATION OF BRANCH BIT EQUAL INSTRUCTION			
1116	*	ROUTINE 07.00	CHECK OPERATION OF BRANCH BIT EQUAL INSTRUCTION			
1117	*	SUB-RTN 07.01	BBE AP,*,1	12	02345	W 02335B 023356 1
1118		BBE		1	02357	.
1119		H	SHOULD BRANCH			
1120	*	SUB-RTN 07.02	TO LOOP. FIX BEFORE PROCEEDING.			
1121		BBE				
1122	AP	BBE	*EB,AQE11,1	12	02358	W 023377 023389 1
1123		B	AQ	7	02370	J 023378
1124		H		1	02377	.
1125	*	SUB-RTN 07.03	SHOULD NOT BRANCH	12	02378	W 023397 023369 1
1126	AQ	BBE	*EB,APQE11,1	7	02390	J 023398
1127		B	AR	1	02397	.
1128		H				
1129	*	SUB-RTN 07.04	SHOULD BRANCH	12	02398	W 024111 02409 2
1130	AR	BBE	AU,*,2	1	02410	.
1131		H				
1132	*	SUB-RTN 07.05	SHOULD NOT BRANCH	12	02411	W 02430 02442 2
1133	AU	BBE	*EB,AXE11,2	7	02423	J 02431
1134		B	AX	1	02430	.
1135	AW	H				
1136	*	SUB-RTN 07.06	SHOULD NOT BRANCH	12	02431	W 02450 024422 8
1137	AX	BBE	*EB,AUC11,8	7	02443	J 02451
1138		B	BA	1	02450	.
1139	AZ	H				
1140	*	SUB-RTN 07.07	SHOULD BRANCH	12	02451	W 02464 02462 4
1141	BA	BBE	BD,*,4	1	02463	.
1142	BC	H				
1143	*	SUB-RTN 07.08	SHOULD NOT BRANCH	12	02464	W 02483 02495 4
1144	BD	BBE	*EB,EGC11,4			

CT ADDRS INSTRUCTION

PGIN	LABEL	CPU TEST	CC01	CPU TEST
	OPCODE	OPERAND	CT	ADDRS
1181	CH	B8E *68,CE11, ^S	12	02643 W 02662 02634 ^S
1182	CK	B CK	7	02655 J 02663
1183	CJ	H	1	02662 *
1184	* SUB-RTN 07.19		12	02663 W 02682 02674
1185	CK	B8E *68,***	7	02675 J 02683
1186		B CN	1	02682 *
1187	CM	H		
1188	* SUB-RTN 07.20		12	02683 W 02702 02714
1189	CN	B8E *68,CQ&11, ^C	7	02695 J 02703
1190		B CQ	1	02702 *
1191	CP	H		
1192	* SUB-RTN 07.21		12	02703 W 02722 02694 ^C
1193	CQ	B8E *68,CN&11, ^C	7	02715 J 02723
1194		B CA	1	02722 *
1195	CS	H		
1196	*****			
1197	*			
1198	* ROUTINE 08.00 CHECK OPERATION OF BRANCH ZONE & BRANCH W/ZONE			
1199	*			
1200	* SUB-RTN 08.01		12	02723 V 02736 09017 2
1201	DA	BZN DD,TPMK.	1	02735 *
1202	DC	H		
1203	* SUB-RTN 08.02		12	02736 V 02755 09032 2
1204	ED	BZN *68,QUOT.	7	02748 J 02756
1205		B DG	1	02755 *
1206	CF	H		
1207	* SUB-RTN 08.03		12	02756 V 02775 09048 2
1208	EG	BZN *68,DELT.	7	02768 J 02776
1209		B CJ	1	02775 *
1210	EI	H		
1211	* SUB-RTN 08.04		12	02776 V 02795 09064 2
1212	EJ	BZN *68,GPMK.	7	02788 J 02796
1213		B DM	1	02795 *
1214	EL	H		
1215	* SUB-RTN 08.05		12	02796 V 02809 09032 S
1216	DM	BZN DP,QUOT,*		

PGLIN	LABEL	CPU TEST		PAGE	INSTRUCTION	
		OPCOD	OPERAND		CT	ADDRS
1217	DO	H			1	02808 .
1218	* SU8-RTN 08.06				12	02809 V 02828 09017 S
1219	DP	8ZN *E8,TPMK,*	DS	SHOULD NOT BRANCH	7	02821 J 02829
1220		8			1	02828 .
1221	CR	H				
1222	* SUB-RTN 08.07				12	02829 V 02848 09048 S
1223	DS	8ZN *E8,DELT,*		SHOULD NOT BRANCH	7	02841 J 02849
1224		8	DV		1	02848 .
1225	DU	H			12	02849 V 02868 09064 S
1226	* SUB-RTN 08.08				7	02861 J 02869
1227	DV	8ZN *E8,GPMK,*		SHOULD NOT BRANCH	1	02868 .
1228		8	DY			
1229	CX	H				
1230	* SUB-RTN 08.09				12	02869 V 02882 09048 K
1231	CY	8ZN EB,DELT,-		SHOULD BRANCH	1	02881 .
1232	EA	H				
1233	* SUB-RTN 08.10				12	02882 V 02901 09017 K
1234	EB	8ZN *E8,TPMK,-		SHOULD NOT BRANCH	7	02894 J 02902
1235		8	EE		1	02901 .
1236	ED	H				
1237	* SUB-RTN 08.11				12	02902 V 02921 09032 K
1238	EE	8ZN *E8,QUOT,-		SHOULD NOT BRANCH	7	02914 J 02922
1239		8	EH		1	02921 .
1240	EG	H				
1241	* SU8-RTN 08.12				7	02934 J 02942
1242	EH	8ZN *E8,GPMK,-		SHOULD NOT BRANCH	1	02941 .
1243		8	EK			
1244	EJ	H				
1245	* SUB-RTN 08.13				12	02942 V 02955 09064 B
1246	EK	8ZN EN,GPMK,&		SHOULD BRANCH	1	02954 .
1247	EM	H				
1248	* SUB-RTN 08.14				12	02955 V 02974 09017 S
1249	EN	8ZN *E8,TPMK,&		SHOULD NOT BRANCH	7	02967 J 02975
1250		8	EQ		1	02974 .
1251	EP	H				

PGLIN	LABEL	CPU TEST	OPCDD	OPERAND	CC01	CPU TEST	CT	ADDR	INSTRUCTION
1252	* SUB-RTN 08.15								
1253	EQ	BZN	*E8,QUOT,E			SHOULD NOT BRANCH			12 02975 V 02994 09032 B
1254		B	ET						7 02987 J 02995
1255	ES	H							1 02994 *
1256	* SUB-RTN 08.16								
1257	ET	BZN	*E8,DELT,E			SHOULD NOT BRANCH			12 02995 V 03014 09048 B
1258		B	EW						7 03007 J 03015
1259	EV	H							1 03014 *
1260	* SUB-RTN 08.17					SHOULD NOT BRANCH			
1261	EW	BWZ	*E8,GPWK,						12 03015 V 03034 09064 3
1262		B	EZ						7 03027 J 03035
1263	EY	H							1 03034 *
1264	* SU8-RTN 08.18								
1265	EZ	BWZ				OPCODE			1 03035 V
1266		DC	FB			I-ADDRESS	*	NOT	5 03040 03054
1267			GMbM			B-ADDRESS	*	BRANCH	5 03045 09071
1268			anA			D-MODIFIER	*		1 03046
1269		B	*E2			SHOULD BRANCH			7 03047 J 03055
1270	FB	H							1 03054 *
1271	*								
1272	* SUB-RTN 10.12					LONG ADD & SUBTRACT USING ALL DIGITS			
1273	HO	Z5	E54321,WORK4-5			WCRK4 SHOULD BE 5432J..... NOW			11 03055 * 09542 09166
1274		Z5	WORK4-5,WORK4			WORK4 SHOULD BE 000005432A NOW			11 03066 * 09166 09171
1275		A	E9876,WORK4-5			WORK4 SHOULD BE 098765432A NDW			11 03077 A 09546 09166
1276		A	E123,WORK4-5			WCRK4 SHOULD BE 099995432A NOW			11 03088 A 09549 09166
1277		A	E45679,WORK4			WCRK4 SHOULD BE 100000000E NDW			11 03099 A 09554 09171
1278		8Z	HP			SHOULD NOT BRANCH			7 03110 J 03219 V
1279		SW	WORK4-8						6 03117 * 09163
1280		Z5	WDRK4						6 03123 * 09171
1281		CW							6 03129 D 09163
1282		BZ	*E8						7 03135 J 03149 V
1283		B	HP						7 03142 J 03219
1284		S	E123,WORK4-5			WDRK4 SHOULD BE 098770000- NOW			11 03149 S 09549 09166
1285		S	-45679,WDRK4			WORK4 SHOULD BE 098765432J NDW			11 03160 S 09559 09171
1286		S	E9876,WORK4-5			WORK4 SHOULD BE 000005432J NOW			11 03171 S 09546 09166

PGLIN	LABEL	CPU TEST OPCODE	C001 OPERAND	CT	ADDRS	INSTRUCTION	CC01	PAGE
1287		S	-54321,WORK4			WORK4 SHOULD BE 00000000- NOW SHOULD BRANCH	11 03182 S 09564 09171	9
1288		BZ	*E8				7 03193 J 03207 V	
1289		B	H-P				7 03200 J 03219	
1290		BZN	HQ,WORK4,-			WILL BRANCH IF ZONED CORRECTLY	12 03207 V 03220 09171 K	
1291		HP	H				1 03219 *	
1292	*	SUB-RTN	10.13	CK B-FIELD ZONE RETENTION & SIGN CHANGE				
1293	HQ	SW	WORK5	PROTECT HI-ORDER FIELD OF WORKS	6 03220	6 09175		
1294		ZA	-1,WORK5	INSURE ZONED NEGATIVELY	11 03226	H 09565 09175		
1295		CW	WORK5	REMOVE WM	6 03237	U 09175		
1296	S	WORK5	*E8,WORK5,-	ZERO OUT WORKS FIELD	6 03243	S 09175		
1297	BZN	HR	*E8,WORK5,-	INSURE	12 03249	V 03268 09175 K		
1298	B	HR	*E8,WORK5-1,+	THAT	7 03261	J 03435		
1299	BZN	HR	*E8,WORK5-1,+	ZONES	12 03268	V 03287 09174 S		
1300	B	HR	*E8,WORK5-2,	ARE	7 03280	J 03435		
1301	BZN	HR	*E8,WORK5-2,	RETAINED	12 03287	V 03306 09173 2		
1302	B	HR	*E8,WORK5-3,+	FOLLOWING	7 03299	J 03435		
1303	BZN	HR	*E8,WORK5-3,+	SINGLE-FIELD	12 03306	V 03325 09172 B		
1304	B	HR	*E8,WORK5-3,+	SUBTRACT	7 03318	J 03435		
1305	A	291Y@,WORK5			11 03325	A 09569 09175		
1306	BZN	HR	*E8,WORK5,6	CHECK	12 03336	V 03355 09175 B		
1307	B	HR	*E8,WORK5-1,+	SIGN	7 03348	J 03435		
1308	BZN	HR	*E8,WORK5-1,+	CHANGE	12 03355	V 03374 09174 S		
1309	B	HR	*E8,WORK5-2,	AND	7 03367	J 03435		
1310	BZN	HR	*E8,WORK5-2,	ZONE	12 03374	V 03393 09173 2		
1311	B	HR	*E8,WORK5-3,+	RETENTION	7 03386	J 03435		
1312	BZN	HR	*E8,WORK5-3,+	FOLLOWING	12 03393	V 03412 09172 B		
1313	B	HR	*E8,WORK5-3,+	ADD	7 03405	J 03435		
1314	S	FIVE9S-1,WORK5		SHOULD CHANGE SIGN BACK TO MINUS	11 03412 S 09252 09175			
1315	BZN	H	*E2,WORK5,-	SHOULD BRANCH	12 03423	V 03436 09175 K		
1316	HR	H			1 03435 *			
1317	*****				*****			
1318	*	ROUTINE	11.00	CHECK OPERATION CLEAR STORAGE				
1319	*	SUB-RTN	11.01	CK CS 0000C FOR NO ERR & PROPER SETTINGS AAR, BAR				
1320	*	SUB-RTN	11.01	CK CS 0000C FOR NO ERR & PROPER SETTINGS AAR, BAR				
1321	*	SUB-RTN	11.01	CK CS 0000C FOR NO ERR & PROPER SETTINGS AAR, BAR				

CC01 CPU TEST
OPCODE OPERAND

PGLIN	LABEL	OPCODE	OPERAND	CC01	INSTRUCTION
1322	HW	CS	0	6	03436 / 00000
1323		SBR	HOLD81-1	7	03442 6 09185 B
1324		SAR	HOLD1	7	03449 6 09181 A
1325		A	60, HOLD1	11	03456 A 09570 09181
1326		BZ	*E8	7	03467 J 03481 V
1327			HX	7	03474 J 03499
1328		S	FIVE9S, HOLD81-1	11	03481 S 09253 09185
1329		B2	HY	7	03492 J 03500 V
1330	HX	H		1	03499 *
1331	*	SUB-RTN	11.02		CHECK PROPER OPERATION CLEAR STORAGE
1332	HY	SW	HZ69	6	INITIALIZE B-FIELD
1333		S	HZ610	6	OF BBE INSTRUCTION
1334		A	FIVE9S-3, HZ610	11	WHICH FOLLOWS
1335		CW	HZ69	6	
1336		SW	201,251	11	
1337		CS	299	6	TRY TO CLEAR 00299 - 00200
1338		BW	JA,251	12	SHOULD NOT BRANCH
1339		BW	JA,201	12	SHOULD NOT BRANCH
1340		SW	201,301	11	PLACE TWO WMS
1341		ZA	E7,201	11	PUT B-A-4-2-1 BITS IN LOC 00201
1342		ZA	E8,301	11	
1343		CW	301,300	11	
1344		ZA	301,300	11	
1345		BBE	JA,201,6	12	
1346		BBE	*E8,201,8	12	
1347		B	JA	7	
1348		CS	299	6	TRY TO CLEAR THE EIGHTS
1349	HZ	88E	JA,299,6	12	BRANCH IF ANY BITS AT ALL
1350		SW	HZ69	6	
1351		S	E1,HZ610	11	
1352		CW	HZ69	6	
1353		B2	JB	7	LEAVE ROUTINE IF NO ERROR
1354		B	H	7	
1355		JA		1	
1356		*			

PGLIN	LABEL	CC01	CPU TEST	CC01	CPU TEST
1392		82	JHEX1	7	03909 J 039 L7 V
1393		H		1	03916 .
1394	* SUB-RTN 13.02		SHOULD BRANCH		
1395	JH	SW	X2-4	6	03917 Q 00030
1396		ZA	*.X2	11	03923 H 03933 00034
1397	S	X2,06X2		11	03934 S 00034 000.0
1398	B2	J16X2	SHOULD BRANCH	7	03945 J 039N3 V
1399	H			1	03952 .
1400	* SUB-RTN 13.03		SHOULD BRANCH		
1401	J1	SW	X3-4	6	03953 Q 00035
1402		ZA	*.X3	11	03959 H 03969 00039
1403	S	X3,06X3		11	03970 S 00039 000M0
1404	B2	JJ6X3	SHOULD BRANCH	7	03981 J 039H9 V
1405	H			1	03988 .
1406	* SUB-RTN 13.04		SHOULD BRANCH		
1407	JJ	SW	X4-4	6	03989 Q 00040
1408		ZA	*.X4	11	03995 H 04005 00044
1409	S	X4,06X4		11	04006 S 00044 00*00
1410	B2	JK6X4	SHOULD BRANCH	7	04017 J 04*25 V
1411	H			1	04024 .
1412	* SUB-RTN 13.05		SHOULD BRANCH		
1413	JK	SW	X5-4	6	04025 Q 00045
1414		ZA	*.X5	11	04031 H 04041 00049
1415	S	X5,06X5		11	04042 S 00049 00*40
1416	B2	JL6X5	SHOULD BRANCH	7	04053 J 04*W1 V
1417	H			1	04060 .
1418	* SUB-RTN 13.06		SHOULD BRANCH		
1419	JL	SW	X6-4	6	04061 Q 00050
1420		ZA	*.X6	11	04067 H 04077 00054
1421	S	X6,06X6		11	04078 S 00054 00*00
1422	B2	JM6X6	SHOULD BRANCH	7	04089 J 04*R7 V
1423	H			1	04096 .
1424	* SUB-RTN 13.07		SHOULD BRANCH		
1425	JH	SW	X7-4	6	04097 Q 00055
1426		ZA	*.X7	11	04103 H 04113 00059

PGLIN	LABEL	CPU TEST		CT	ADDRS	INSTRUCTION	CC01	PAGE	13
		OPCODE	OPERAND						
1427		S	X7,06X7				11	04114	S 00059 00* ^Q 0
1428		BZ	JNEX7				7	04125	J 04/C3 V
1429		H					1	04132	.
1430	* SUB-RTN 13.08						6	04133	0 00060
1431	JN	SW	X8-4				11	04139	Q 04149 00064
1432		ZA	* ,X8				11	04150	S 00064 00.00
1433		S	X8,06X8				7	04161	J 04J69 V
1434		BZ	JPEX8				1	04168	.
1435		H							
1436	* SUB-RTN 13.09						6	04169	0 00065
1437	JP	SW	X9-4				11	04175	Q 04185 00069
1438		ZA	* ,X9				11	04186	S 00069 00.00
1439		S	X9,06X9				7	04197	J 04K*5 V
1440		BZ	JQE X9				1	04204	.
1441		H							
1442	* SUB-RTN 13.10						6	04205	0 00070
1443	JQ	SW	X1C-4				11	04211	Q 04221 00074
1444		ZA	* ,X10				11	04222	S 00074 00.00
1445		S	X1C,06X10				7	04233	J 04KML V
1446		BZ	JRCX10				1	04240	.
1447		H							
1448	* SUB-RTN 13.11						6	04241	0 00075
1449	JR	SW	X11-4				11	04247	Q 04257 00079
1450		ZA	* ,X11				11	04258	S 00079 00.00
1451		S	X11,06X11				7	04269	J 04KG7 V
1452		BZ	JSEX11				1	04276	.
1453		H							
1454	* SUB-RTN 13.12						6	04277	0 00080
1455	JS	SW	X12-4				11	04283	Q 04293 00084
1456		ZA	* ,X12				11	04294	S 00084 00M00
1457		S	X12,06X12				7	04305	J 04C13 V
1458		BZ	JTEX12				1	04312	.
1459		H							
1460	* SUB-RTN 13.13						6	04313	0 00085
1461	JT	SW	X13-4				11	04319	Q 04329 00089
1462		ZA	* ,X13						

PGLIN	LABEL	CPU TEST	CC01	CT	ADDR	INSTRUCTION
1463	S	X13,06X13	11	04330	S	00089 00H*0
1464	BZ	JUEX13	7	04341	J	04CU9 V
1465	H		1	04348	*	
1466	* SUB-RTN 13.14					
1467	JU	SW	6	04349	J	00090
1468		ZA	11	04355	H	04365 0094
1469		S	11	04366	S	00094 00H.0
1470		BZ	7	04377	J	04CQ5 V
1471	H		1	04384	*	
1472	* SUB-RTN 13.15					
1473	JV	SW	6	04385	J	00095
1474		ZA	11	04391	H	04401 00099
1475		S	11	04402	S	00099 00MHO
1476		BZ	7	04413	J	04DB1 V
1477	H		1	04420	*	
1478	*****					
1479	*					
1480	* ROUTINE 15.00	CHECK OPERATION OF BRANCH CHARACTER EQUAL				
1481	*					
1482	* SUB-RTN 15.01	COMPARE D-MOD 9 WITH B-FLD 3 FOR LO COMPARE				
1483	*	ANC NO BRANCH. CHECK AAR & BAR SETTINGS				
1484	KFO1	BCE	12	04421	B	04504 090B7 9
1485		SAR	7	04433	C	09181 A
1486		SBR	7	04440	G	09186 B
1487		BL	7	04447	J	04461 T
1488		KFC2	7	04454	J	04504
1489		EKF02,HOLDA2	11	04461	S	09593 09181
1490	BZ	*E8	7	04472	J	04486 V
1491	B	KFC2	7	04479	J	04504
1492	S	EPCUND,HOLDB2	11	04486	S	09598 09186
1493	BZ	KFC3	7	04497	J	04505 V
1494	KFO2	H	1	04504	*	
1495	* SUB-RTN 15.02	COMPARE D-MOD AT SIGN WITH B-FLD NINE				
1496	*	FOR HI COMPARE AND NO BRANCH.				
1497	KFO3	BCE	12	04505	B	04538 09129 3
1498	BR	*E8	7	04517	J	04531 U

PGLIN	LABEL	CC01 CPU TEST OPCODE OPERAND	CC01 CPU TEST OPCODE OPERAND	CT ADDRS	INSTRUCTION	PAGE 15
1499		B *68			7 04524 J 04538	
1500		B- KFCS			7 04531 J 04539 U	
1501	KF04	H			1 04538 *	
1502	* SUB-RTN 15.03	COMPARE D-MOD AMPERSAND W/B-FLD AMPERSAND FOR EQ COMPARE AND BRANCH. CHECK AAR & BAR SETTINGS				
1503	*					
1504	KF05	BCE KF07,AMPSND,6	SHOULD BRANCH			
1505	KF06	B KF08			7 04551 J 04636	
1506	KF07	SAR HOLD A2			7 04558 G 09181 A	
1507		SBR HDLCB2			7 04565 G 09186 B	
1508		BU KF08	SHOULD NOT BRANCH		7 04572 J 04636 /	
1509		BE *68	SHOULD BRANCH		7 04579 J 04593 S	
1510		B KFC8			7 04586 J 04636	
1511		S EKF07,HOLDA2			11 04593 S 09603 09181	
1512		BZ *68			7 04604 J 04618 V	
1513		B KFC8			7 04611 J 04636	
1514		S EKF06,HOLD B2	SHOULD BRANCH & EXIT		11 04618 S 09608 09186	
1515		BZ KG			7 04629 J 04637 V	
1516	KF08	H			1 04636 *	
1517		*****				
1518	*					
1519	*	ROUTINE 16.00	CHECK CERTAIN MOVE OPCODES PREPARATORY TO COMPARE			
1520	*					
1521	* SUB-RTN 16.01	CHECK SCNLS FOR STEPPING AAR, BAR ONE POSITION				
1522	KG	CS 103			6 04637 / 00103	
1523		SCNLS 102,103			12 04643 0 00102 00103	
1524		SAR HOLD A2			7 04655 G 09181 A	
1525		SBR HOLD B2			7 04662 G 09186 B	
1526		S A0C101A,HOLDA2	SHOULD BRANCH		11 04669 S 09613 09181	
1527		BZ *68			7 04680 J 04694 V	
1528		B KH			7 04687 J 04712	
1529		S A0C102A,HOLD B2	SHOULD BRANCH		11 04694 S 09618 09186	
1530		BZ K1			7 04705 J 04713 V	
1531	KH	H			1 04712 *	
1532	* SUB-RTN 16.02	CHECK MLNS FOR CORRECT OPERATION				
1533	KI	CS 101			6 04713 / 00101	
1534		SW 10C			6 04719 , 00100	

CC01 PAGE 17
CT ADORS INSTRUCTION

CC01 CPU TEST
OPCOD OPERAND

PGLIN

LABEL

1571 * THIS ROUTINE COMPARES ALL SIXTY-FOUR LEGITIMATE
1572 * CHARACTERS WITH ONE ANOTHER AND INSURES THAT ALL
1573 * IDENTICAL CHARACTERS COMPARE EQUAL. THAT NO
1574 * CHARACTER COMPARES EQUAL TO ANY CHARACTER EXCEPT
1575 * ITSELF, AND THAT THE COLLATING SEQUENCE IS PROPER

1576 *

1577 * BEGIN BY USING SIMPLEST COMPARISONS TO VERIFY
1578 * CORRECT OPERATION OF BRANCH HI, LO, EQ, UNEQUAL

1579 *

* SUB-RTN 17.01 COMPARE A-FLD 9 WITH B-FLD 3 FOR LO COMPARE

1580 KR C NINE,ATSIGN	1581 KR 8E KS SHOULD NOT BRANCH	1582 BU *68 SHOULD BRANCH	1583 B KS	1584 B *68 SHOULD NOT BRANCH	1585 BF KT SHOULD BRANCH	1586 BL H	1587 KS H
* SUB-RTN 17.02 COMPARE A-FLD 3 WITH B-FLD 9 FOR HI COMPARE	KT C ATSIGN,NINE	KU SHOULD NOT BRANCH	BU *68 SHOULD BRANCH	B KU	BL KU	BF KV	KU H
1588	1589	1590	1591	1592	1593	1594	1595

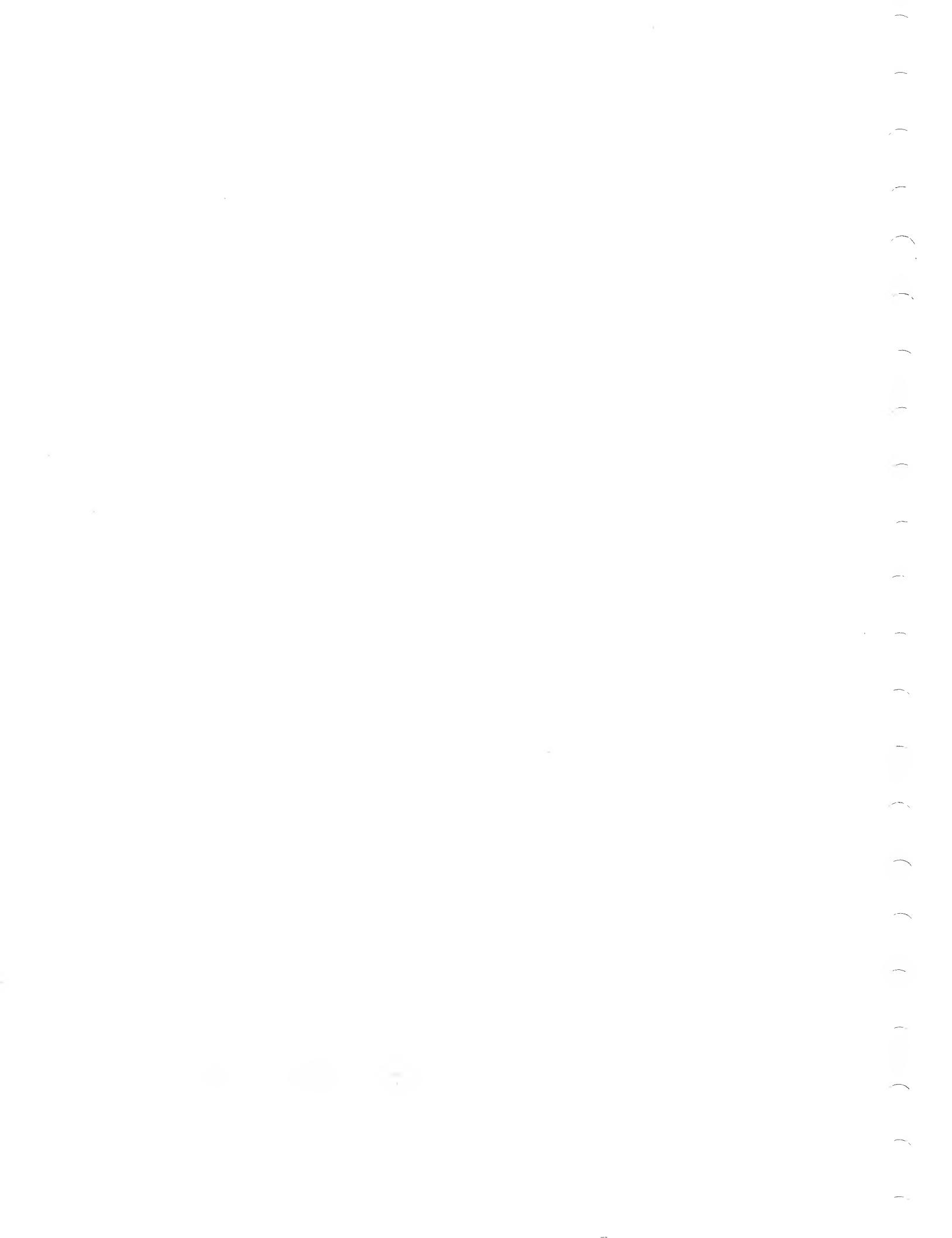
1596 *

* SUB-RTN 17.03 COMPARE AMPSAND WITH AMPSAND FOR EQ COMPARE

1597 KV C AMPSNO,AMPSND	1598 BU KW SHOULD	1599 BF KW NOT	1600 BL KW BRANCH	1601 BE *62 SHOULD BRANCH	1602 KW H	1603 *****	1604 * ROUTINE 19.00 CHECK OPERATION OF DATA MOVE INSTRUCTION	1605 *
11 05005 C 09129 09087	7 05016 J 05051 S	7 05023 J 05037 /	7 05030 J 05051	7 05037 J 05051 U	7 05044 J 05052 T	1 05051 *	11 05052 C 09087 09129	7 05063 J 05098 S
11 05070 J 05084 /	7 05077 J 05098	7 05084 J 05098 T	7 05091 J 05099 U	1 05098 *	11 05099 C 09072 09072	7 05110 J 05138 /		
7 05117 J 05138 U	7 05124 J 05138 T	7 05131 J 05139 S	1 05138 *	7 05110 J 05138 /				

1606	*	SUB-RTN	19.01	CHECK SCNLS FOR MOVE NO DATA	
1607	LK	MLCS	NWM63,WORK6		12 05139 D 09064 09176 3
1608	SW	WORK6		6 05151 * 09176	
1609	SCNLS	NWM00,WORK6		12 05157 D 09002 09176	
1610	C	ALLBIT,WORK6		11 05169 C 09071 09176	
1611	BE	LL	SHOULD BRANCH	7 05180 J 05188 S	
1612	H			1 05187 *	
1613	*	SUB-RTN	19.02	CHECK MLNS FOR MOVE NUMERIC, NO ZONES, NO WM	
1614	LL	MLCS	NWM62,WORK6		12 05188 D 09063 09176 3
1615	SW	WORK6		6 05200 * 09176	
1616	MLNS	NWM01,WORK6		12 05206 D 09003 09176 1	
1617	C	AYE,WORK6		11 05218 C 09092 09176	
1618	BE	LM	SHOULD BRANCH	7 05229 J 05237 S	
1619	H			1 05236 *	
1620	*	SUB-RTN	19.03	CHECK MLZS FOR MOVE ZONES, NO NUMERIC, NO WM	
1621	LH	MLCS	NWM31,WORK6		12 05237 D 09032 09176 3
1622	SW	WORK6		6 05249 * 09176	
1623	MLZS	NWM32,WORK6		12 05255 D 09033 09176 2	
1624	C	DELTA,WORK6		11 05267 C 09077 09176	
1625	BE	LN	SHOULD BRANCH	7 05278 J 05286 S	
1626	H			1 05285 *	
1627	*	SUB-RTN	19.04	CHECK MLCS FOR MOVE NUMERIC, ZONE, NO WM	
1628	LN	MLNS	NWM25,WORK6		12 05286 D 09027 09176 1
1629	MLZS	NWM25,WORK6		12 05298 D 09027 09176 2	
1630	SW	WORK6		6 05310 * 09176	
1631	MLCS	NWM38,WORK6		12 05316 D 09039 09176 3	
1632	C	OH,WORK6		11 05328 C 09107 09176	
1633	BE	LP	SHOULD BRANCH	7 05339 J 05347 S	
1634	H			1 05346 *	
1635	*	SUB-RTN	19.05	CHECK MLWS FOR MOVE WM, NO ZONE, NO NUMERIC	
1636	LP	MLCS	NWM63,WORK6		12 05347 D 09064 09176 3
1637	CW	WORK6		6 05359 * 09176	
1638	MLWS	BLANK,WORK6		12 05365 D 09066 09176 4	
1639	C	ALLBIT,WORK6		11 05377 C 09071 09176	
1640	BE	LQ	SHOULD BRANCH	7 05388 J 05396 S	
1641	H			1 05395 *	
1642	*	SUB-RTN	19.06	CHECK MLNWS FOR MOVE NUMERIC, WM, NO ZONE	
1643	LQ	MLCS	NWM54,WORK6		12 05396 D 09054 09176 1
1644	A	WORK6		6 0 J8 L 09176	

1645	PLNHS	NINE,MDRK6	12	05414	D 09129 09176 5	
1646	C	EYE,WORK6	11	05426	C 09100 09176	
1647	BE	LR	SHOULD BRANCH	7	05437	J 05445 S
1648	H			1	05444	*
1649	*	SUB-RTN 19.07	CHECK MLZWS FOR MOVE ZONE, WM, NO NUMERIC	12	05445	D 09032 09176 3
1650	LR	MLCS	NWM31,WORK6	6	05457	□ 09176
1651	CW	WORK6		12	05463	D 09078 09176 6
1652	MLZWS	DASH,WORK6		11	05475	C 09077 09176
1653	C	DELTA,WORK6		7	05486	J 05494 S
1654	BE	LS	SHOULD BRANCH	1	05493	*
1655	H			12	05494	D 09002 09176 3
1656	*	SUB-RTN 19.08	CHECK MLCWS FOR MOVE CHARACTER AND WORD MARK	6	05506	□ 09176
1657	LS	MLCS	NWM00,WORK6	12	05512	D 09071 09176 7
1658	CW	WORK6		11	05524	C 09071 09176
1659	MLCWS	ALLBIT,WORK6		7	05535	J 05543 S
1660	C	ALLBIT,MDRK6		1	05542	*
1661	BE	LT	SHOULD BRANCH	12	05543	0 09064 00100 7
1662	H			12	05555	D 09066 00101 7
1663	*	SUB-RTN 19.09	CHECK SCNR FOR MOVE NO DATA, PROPER ADDR REG STEP	12	05567	D 00100 00101 8
1664	LT	MLCWS	NWM63,100	7	05579	G 09181 A
1665	MLCWS	BLANK,101		7	05586	G 09186 B
1666	SCNR	LOC,101		11	05593	C 09181 09613
1667	SAR	HOLDA2		7	05604	J 05709 /
1668	SBR	HOLDB2		11	05611	C 09186 09618
1669	C	HOLDA2,00010101	CK AAR FOR PROPER STEPPING	7	05622	J 05709 /
1670	BU	LU	SHOULD NDT BRANCH	11	05629	C 09066 00101
1671	C	HOLDB2,00010201	CK BAR FOR PROPER STEPPING	7	05640	J 05709 /
1672	BU	LU	SHOULD NDT BRANCH	12	05647	D 00101 00100 8
1673	C	BLANK,101	TEST LOC 00101 FDR WM-BLANK	7	05659	G 09181 A
1674	BU	LU	SHOULD NOT BRANCH	7	05666	G 09186 B
1675	SCNR	101,100		11	05673	C 09181 09618
1676	SAR	HOLDA2		7	05684	J 05709 /
1677	SBR	HOLDB2		11		



PGLIN	LABEL	CPU TEST		CC01	PAGE 19	
		OPCOD	OPERAND			
1685		MRN	COLON, WORK6	12	05722	D 09088 09176 9
1686		BW	*E13, WORK6	12	05734	V 05758 09176 1
1687		BCE	LW, WORK6, B	12	05746	B 05759 09176 B
1688	H			1	05758	.
1689	* SUB-RTN 19.11		CHECK MRZ	12	05759	D 09048 09176 7
1690	LW	MLCWS	NW#47, WORK6	12	05771	D 09085 09176 0
1691		MRZ	SUELNK, WORK6	12	05783	V 05807 09176 1
1692	BW	*E13, WORK6		12	05795	B 05808 09176 S
1693	BCE	LX, WORK6, M		1	05807	.
1694	H					
1695	* SUB-RTN 19.12		CHECK MRC	12	05808	D 09014 09176 7
1696	LX	MLCWS	NW#12, WORK6	12	05820	D 09094 09176 #
1697		MRC	SEE, WORK6	12	05832	V 05856 09176 1
1698	BW	*E13, WORK6	SHOULD NOT BRANCH	12	05844	B 05857 09176 C
1699	RCE	LY, WORK6, C	SHOULD BRANCH	1	05856	.
1700	H					
1701	* SUB-RTN 19.13		CHECK MRW	12	05857	D 09071 09176 7
1702	LY	MLCWS	ALLBIT, WORK6	12	05869	D 09002 09176 3
1703		MRW	NW#00, WORK6	12	05881	V 05905 09176 1
1704	BW	*E13, WORK6	SHOULD NOT BRANCH	12	05893	B 05906 09176 G
1705	BCF	LZ, WORK6, M	SHOULD BRANCH	1	05905	.
1706	H					
1707	* SUB-RTN 19.14		CHECK MRNW	12	05906	D 09091 09176 7
1708	LZ	MLCWS	QUESTN, WORK6	12	05918	D 09007 09176 .
1709		MRNW	NW#05, WORK6	12	05930	V 05954 09176 1
1710	BW	*E13, WORK6	SHOULD NOT BRANCH	12	05942	B 05955 09176 E
1711	RCE	MA, WORK6, E	SHOULD BRANCH	1	05954	.
1712	H					
1713	* SUB-RTN 19.15		CHECK MRZW	12	05955	D 09090 09176 7
1714	PA	MLCWS	TPMARK, WORK6	12	05967	D 09049 09176 G
1715		MRZWM	NW#48, WORK6	12	05979	V 06003 09176 1
1716	BW	*E13, WORK6		12	05991	B 06004 09176 H
1717	BCE	MR, WORK6, M		1	06003	.
1718	H					
1719	* SUB-RTN 19.16		CHECK MRZW			

PGLIN	LABEL	CPU TEST	OPCODE	OPERAND
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PGLIN	LABEL	CPU TEST	OPCODE	OPERAND	CT	ADDR	INSTRUCTION	
1720	MB	MLCWS	EPY, WORK6		12	06004	D 09105 09176 7	
1721		MRCW	NWM27, WORK6		12	06016	D 09028 09176 M	
1722		BW	*E13, WORK6	SHOULD NOT BRANCH	12	06028	V 06052 09176 1	
1723		BCE	MC, WORK6, *	SHOULD BRANCH	12	06040	B 06053 09176 *	
1724	H				1	06052	*	
1725		* SUB-RTN 19.17 CHECK SCNLA FOR MOVE NO DATA, PROPER ADDR REG STEP				12	06053	D 09069 00102 7
1726	MC	MLCWS	LBRAKT, 102		12	06065	D 09004 00103 7	
1727		MLCWS	NWM02, 103		12	06077	D 09069 00104 7	
1728		MLCWS	LBRAKT, 1C4		12	06089	D 00103 00104 5	
1729		SCNLA	103, 104		7	06101	G 09181 A	
1730		SAR	HOLDA2		7	06108	G 09186 B	
1731		SBR	HOLD82		11	06115	C 09181 09613	
1732		C	HOLDA2, 00010101	CHECK AAR FOR PROPER STEPPING	7	06126	J 06169 /	
1733		BU	MD	SHOULD NOT BRANCH	11	06133	C 09186 09618	
1734		C	HOLD82, 00010202	CHECK BAR FOR PROPER STEPPING	7	06144	J 06169 /	
1735		BU	MD	SHOULD NOT BRANCH	11	06151	C 09062 00104	
1736		C	NWM61, 104	TEST THAT NO DATA WERE MOVED	7	06162	J 06170 \$	
1737		BE	ME	SHOULD BRANCH & EXIT	1	06169	*	
1738	MD	H			1	06169	*	
1739		* SUB-RTN 19.18 CHECK MLNA				12	06170	D 09077 00102 7
1740	ME	MLCWS	DELTA, 102		12	06182	D 09018 00103 7	
1741		MLCWS	NWM16, 103		12	06194	D 09077 00104 7	
1742		MLCWS	DELTA, 104		12	06206	D 00103 00104 /	
1743		MLNA	103, 104		11	06218	C 09033 00104	
1744		C	NWM32, 104		7	06229	J 06237 S	
1745		BE	MF	SHOULD BRANCH & EXIT	1	06236	*	
1746	H				1	06236	*	
1747		* SUB-RTN 19.19 CHECK MLZA				12	06237	D 09081 00102 7
1748	MF	MLCWS	PERCNT, 102		12	06249	D 09036 00103 7	
1749		MLCWS	NWM35, 103		12	06261	D 09081 00104 7	
1750		MLCWS	PERCNT, 104		12	06273	D 00103 00104 S	
1751		MLZA	103, 104		11	06285	C 09045 00104	
1752		C	NWM44, 104		7	06296	J 06304 S	
1753		BE	MG	SHOULD BRANCH & EXIT	1	06303	*	
1754	H							

PGLIN	LABEL	CPU TEST	CC01	CPU TEST	CC01	PAGE 21
		OPCOD	OPCOD	OPERAND	ADDR	INSTRUCTION
1755	*	SUB-RTN 19.20	CHECK MLCWA			
1756	MIG	MLCWS	NWM63,WORK6		12 06304 0 09064 09176 7	
1757		MLCA	BLANK,WORK6		12 06316 D 09066 09176 1	
1758		BW	*613,WORK6	SHDULD NOT BRANCH	12 06328 V 06352 09176 1	
1759		BCE	MH,WORK6,	SHDULD BRANCH	12 06340 B 06353 09176	
1760		H			1 06352 *	
1761	*	SUB-RTN 19.21	CHECK MLWA			
1762	MH	MLCWS	NWM53,WORK6		12 06353 0 09054 09176 7	
1763		MLWA	NAUGHT,WORK6		12 06365 0 09120 09176 U	
1764		C	NWM53,WORK6	SHDULD BRANCH	11 06377 C 09054 09176	
1765		BE	M1		7 06388 J 06396 S	
1766		H			1 06395 *	
1767	*	SUB-RTN 19.22	CHECK MLNWA			
1768	M1	MLCWS	NWM47,WORK6		12 06396 0 09048 09176 7	
1769		MLNWA	SUBLNK,WORK6		12 06408 D 09085 09176 V	
1770		C	NWM32,WORK6	SHDULD BRANCH	11 06420 C 09033 09176	
1771		BE	MJ		7 06431 J 06439 S	
1772		H			1 06438 *	
1773	*	SUB-RTN 19.23	CHECK MLZWA			
1774	MJ	MLCWS	NWM03,WORK6		12 06439 D 09005 09176 7	
1775		MLZWA	LDZNGE,WORK6		12 06451 D 09068 09176 W	
1776		C	NWM51,WRK6	SHDULD BRANCH	11 06463 C 09052 09176	
1777		BE	MK		7 06474 J 06482 S	
1778		H			1 06481 *	
1779	*	SUB-RTN 19.24	CHECK MLCWA			
1780	MK	MLCWS	ALLBIT,102		12 06482 D 09071 00102 7	
1781		MLCWS	NWM00,103		12 06494 0 09002 00103 7	
1782		MLCWS	ALLBIT,104		12 06506 D 09071 00104 7	
1783		MLCWA	103,104	SHDULD NOT BRANCH	12 06518 D 00103 00104 X	
1784		BW	*613,104		12 06530 V 06554 00104 1	
1785		BCE	ML,104,	SHDULD BRANCH	12 06542 B 06555 00104	
1786		H			1 06554 *	
1787	*	SUB-RTN 19.25	CHECK SCNRR FOR MOVE NO DATA, PROPER ADDR REG STP			
1788	MJ	MLCWA	NWM26,101		12 06555 D 09065 00101 X	
1789		MLCWS	GREATR,37		12 06567 D 09089 00037 7	

CC01 CPU TEST
OPCODE OPERAND

CT ADDRS INSTRUCTION

PGLIN	LABEL	MLCWS	NWM49.36	12	06579	D 09050 00036 7
1790	SCNRR	37.36		12	06591	D 00037 00036 Y
1791	SAR	HOLDA2		7	06603	G 09181 A
1792	S8R	HOLDB2		7	06610	G 09186 B
1793	C	HOLDA2,300102a	CHECK AAR FOR PROPER STEPPING	11	06617	C 09181 09618
1794	BU	MM	SHOULD NOT BRANCH	7	06628	J 06677 /
1795	C	HOLDB2,300101a	CHECK BAR FOR PROPER STEPPING	11	06635	C 09186 09613
1796	BU	MM	SHOULD NOT BRANCH	7	06646	J 06677 /
1797	SW	38		6	06653	• 00038
1798	C	NWM26,101	TEST THAT NO DATA WERE MOVED	11	06659	C 09065 00101
1799	BE	NN	SHOULD BRANCH & EXIT	7	06670	J 06678 S
1800	MM	H		1	06677	•
1801	* SUB-RTN 19.26	CHECK MRNR		6	06678	n 00100
1802	PN	CW	10C	12	06684	D 09130 00100 M
1803	MRCW	K01.100		12	06696	D 09132 00100 L
1804	MRNR	K02.100		12	06708	V 06770 00100 1
1805	MP	MP.100	SHOULD NOT BRANCH	12	06720	V 06739 00101 1
1806	BW	*E8.101	SHOULD BRANCH	7	06732	J 06770
1807	BW	MP	SHOULD BRANCH	12	06739	B 06758 00100
1808	B	BCE	*E8.100,	7	06751	J 06770
1809	B	MP		12	06758	B 06771 00101 :
1810	BCE	MQ.101.:		1	06770	•
1811	P	H		6	06771	n 00100
1812	* SUB-RTN 19.27	CHECK MRZR		12	06777	D 09134 00100 M
1813	PQ	CW	100	12	06789	D 09136 00100 *
1814	MRCW	KC3.100		12	06801	V 06863 00100 1
1815	MRZR	K04.100	SHOULD NOT BRANCH	12	06813	V 06832 00101 1
1816	MR	MR.100	SHOULD BRANCH	7	06825	J 06863
1817	BW	*E8.101	SHOULD BRANCH	12	06832	B 06851 00100 -
1818	B	MR		7	06844	J 06863
1819	BCE	*E8.100,-		12	06851	B 06864 00101 V
1820	B	MR		1	06863	•
1821	BCE	MS.101.V	SHOULD BRANCH & EXIT			
1822	MR	H				
1823	* SUB-RTN 19.28	CHECK MRCR				
1824						

PGLIN LABEL CPU TEST
OPCODE OPERAND

PGLIN	LABEL	CC01	CPU TEST	CC01	PAGE 23
		OPCODE	OPERAND	INSTRUCTION	
1825	MS	MLCWA	K05,101		
1826		MRCR	K06,100		
1827		BW	*E8,100	SHOULD BRANCH	
1828		PT	8		
1829		C	101,K1461		
1830		BE	M11	SHOULD BRANCH & EXIT	
1831	PT	H			
1832		* SUB-RTN 19.29	CHECK MRWR		
1833	MU	MLCWA	K07,101		
1834		MRWR	K08,100	SHOULD NOT BRANCH	
1835		BW	MV,100	SHOULD BRANCH	
1836		8W	*E8,101	SHOULD BRANCH	
1837		8	MV		
1838		BCE	*E8,100,I	SHOULD BRANCH	
1839		8	MV		
1840		8CE	MW,101,N	SHOULD BRANCH & EXIT	
1841	MV	H			
1842		* SUB-RTN 19.30	CHECK MRNWR		
1843	MW	MLCWA	K09,101		
1844		MRNWR	K1C,100	SHOULD NOT BRANCH	
1845		BW	MX,100	SHOULD BRANCH	
1846		8W	*E8,101	SHOULD BRANCH	
1847		8	MX		
1848		8CE	*E8,100,S	SHOULD BRANCH	
1849		8	MX		
1850		8CE	MY,101,?		
1851	MX	H			
1852		* SUB-RTN 19.31	CHECK MRZWR		
1853	MY	MLCWA	K11,101		
1854		MRZWR	K12,100	SHOULD NOT BRANCH	
1855		8W	MZ,100	SHOULD BRANCH	
1856		8W	*E8,101	SHOULD BRANCH	
1857		8	MZ		
1858		BCE	*E8,100,X	SHOULD BRANCH	
1859		6	MZ		

PGLIN	LABEL	CC01	CPU TEST	CC01	CPU TEST
1860		8CE	NA,101,V	SHOULD BRANCH & EXIT	12 07174 B 07187 00101 V
1861	H		CHECK MRCWR		1 07186 *
1862	* SUB-RTN 19.32				
1863	NA	CW	100		6 07187 □ 00100
1864		MRCW	K13,100		12 07193 D 09154 00100 H
1865		MRCWR	K14,100		12 07205 D 09156 00100 S
1866		8W	*68,100	SHOULD BRANCH	12 07217 V 07236 00100 1
1867		B	NB		7 07229 J 07254
1868		C	101,K1461		11 07236 C 00101 09157
1869		AE	NC	SHOULD BRANCH & EXIT	7 07247 J 07255 S
1870	H				1 07254 *
1871	* SUB-RTN 19.33	CHECK SCNLB FOR MOVE NO DATA, PROPER ADDR REG STP			
1872	NC	MLCWS	TPMARK,1C2		12 07255 D 09090 00102 7
1873		MLCWS	NWM48,103		12 07267 D 09049 00103 7
1874		MLCWS	AMPSND,104		12 07279 D 09072 00104 7
1875		SCNLB	104,103		12 07291 D 00104 00103 -
1876		SAR	HOLDA2		7 07303 G 09181 A
1877		S8R	HOLDB2		7 07310 G 09186 B
1878		C	HOLDA2,300102A		11 07317 C 09181 09618
1879		ND		SHOULD NOT BRANCH	7 07328 J 07371 /
1880		C	HOLDB2,300101A		11 07335 C 09186 09613
1881		BU	ND	SHOULD NOT BRANCH	7 07346 J 07371 /
1882		C	NWM15,102	TEST THAT NO DATA WERE MOVED	11 07353 C 09017 00102
1883		8E	NE	SHOULD BRANCH & EXIT	7 07364 J 07372 S
1884	NO	H			1 07371 *
1885	* SUB-RTN 19.34	CHECK MLNB			
1886	NE	MLCWS	BKSLSH,WORK6		12 07372 D 09083 09176 7
1887		MLNB	NWM33,WORK6		12 07384 D 09034 09176 J
1888		C	NWM17,WORK6		11 07396 C 09019 09176
1889		BE	NF	SHOULD BRANCH	7 07407 J 07415 S
1890		H			1 07414 *
1891	* SUB-RTN 19.35	CHECK MLZB			
1892	NF	SW	10C		6 07415 * 00100
1893		MLCWS	NWM63,101		12 07421 D 09064 00101 7
1894		MLZB	BLANK,101		12 07433 D 09066 00101 K

PGLIN	LABEL	CPU TEST	OPCOD	OPERAND	CT	ADDRS	INSTRUCTION
1895		BW *E13,1C1			12	07445	V 07469 00101 1
1896		8CE NG,101,M			12	07457	8 07470 00101 M
1897		H			1	07469	*
1898	* SUB-RTN 19.36	CHECK MLCB			6	07470	*
1899	NG	SW 10C	MLCWS	NW#52,101	12	07476	0 09053 00101 7
1900		MLCWS	NW#52,101		12	07488	D 09086 00101 L
1901		MLC8	POUN0,101		12	07500	V 07524 00101 1
1902		BW *E13,1C1			12	07512	B 07525 00101 *
1903		BCE NH,101,#			1	07524	*
1904		H					
1905	* SUB-RTN 19.37	CHECK MLWB			6	07525	*
1906	NH	SW 10C	MLCWS	NW#15,101	12	07531	D 09017 00101 7
1907		MLCWS	NW#15,101		12	07543	D 09072 00101 M
1908		MLWB	AMPSN0,101		11	07555	C 09017 00101
1909		C	NW#15,101		7	07566	J 07574 S
1910	④	BE NI			1	07573	*
1911		H					
1912	* SUB-RTN 19.38	CHECK MLNWB			6	07574	*
1913	NJ	SW 10C	MLCWS	NW#06,101	12	07580	D 09008 00101 7
1914		MLCWS	NW#06,101		12	07592	D 09100 00101 N
1915		MLNWB	EYE,101		11	07604	C 09011 00101
1916		C	NW#09,101		7	07615	J 07623 S
1917	④	BE NJ			1	07622	*
1918		H					
1919		* SUB-RTN 19.39	CHECK MLZWB		12	07623	D 09071 09176 7
1920	NJ	MLCWS	ALL81T,WORK6		12	07635	D 09002 09176 0
1921		MLZWB	NW#00,WORK6		12	07647	V 07671 09176 1
1922		BW *E13,WORK6			12	07659	B 07672 09176 M
1923		BCE NK,WORK6,M			1	07671	*
1924		H					
1925	* SUB-RTN 19.40	CHECK MLCWB			12	07672	D 09068 09176 7
1926	NK	MLCWS	LOZNGE,WORK6		12	07684	D 09005 09176 P
1927		MLCWB	NW#03,WORK6		12	07696	V 07720 09176 1
1928		BW *E13,WORK6			12	07708	B 07721 09176 3
1929		8CE NL,WORK6,3					

PGLIN

LABEL

CT ADDRS INSTRUCTION

CC01

CPU TEST

OPCODE OPERAND

PGLIN	LABEL	CT	ADDRS	INSTRUCTION
1930		1	07720	*
1931	H	• SUB-RTN 19.41	CHECK SCNRG FOR MOVE NO DATA, PROPER ACDR REG STP	
1932	NL	CS 164	INSURE 00100-00164 BLANK	6 07721 / 00164
1933		MLCWS ALLBIT,101	PUT TERMINAL CHARACTER IN 00101	12 07727 D 09071 00101 7
1934		MLWA 164,100	INSURE NO WMS 00038-00100	12 07739 D 00164 00100 U
1935		MLCWB NINE,100	MOVE 64 CHARACTERS TO 00037-00100	12 07751 D 09129 00100 P
1936	CW	42	REMOVE WM FROM GROUP MARK	6 07763 □ 00042
1937		SCNRG 37,36	TRY THE SCAN	12 07769 D 00037 00036 Q
1938	SAR	HOLDA2		7 07781 G 09181 A
1939	S8R	HOLDB2		7 07788 G 09186 B
1940	C	HOLDA2,AC0102a	CHECK AAR FOR PROPER SETTING	11 07795 C 09181 0961B
1941	RU	NM	SHOULD NOT BRANCH	7 07806 J 07885 /
1942	C	HOLDB2,AC00101a	CHECK BAR FOR PROPER SETTING	11 07813 C 09186 09613
1943	BU	NM	SHOULD NOT BRANCH	7 07824 J 07885 /
1944	BW	NM,42	SHOULD NOT BRANCH	12 07831 V 07885 00042 1
1945	MLWA	164,100	REMOVE ALL WMS FROM 00038-00100	12 07843 0 00164 00100 U
1946	MLCB	NINE,164	MOVE 64 CHARACTERS TO 00101-00164	12 07855 D 09129 00164 L
1947	C	100,164	CHECK THAT SCAN MOVED NO DATA	11 07867 C 00100 00164
1948	BE	NN	SHOULD BRANCH	7 07886 J 07886 S
1949	NN	H		1 07885 *
1950	H	• SUB-RTN 19.42	CHECK MRNG	
1951	NN	MLCWS NW#19,101		12 07886 D 09021 00101 7
1952		MLCWS SPLAT,102		12 07898 D 09074 00102 7
1953		MLCWS ALLBIT,103		12 07910 D 09071 00103 7
1954		MRNG 102,101		12 07922 D 00102 00101 R
1955	8W	*E13,1C1	SHOULD NOT BRANCH	12 07934 V 07958 00101 1
1956	BCE	NP,101,8		12 07946 B 07959 00101 Z
1957		H		1 07958 *
1958	H	• SUB-RTN 19.43	CHECK MRZG	
1959	NP	MLCWS ALLBIT,101		12 07959 D 09071 00101 7
1960		MLCWS NW#00,102		12 07971 D 09002 00102 7
1961		MLCWS ALLBIT,103		12 07983 D 09071 00103 7
1962		MRZG 102,101		12 07995 D 00102 00101 *
1963	C	NW#15,101		11 08007 C 09017 00101
1964	BE	NQ	SHOULD BRANCH	7 0801B J 08026 S

PGLIN	LABEL	CC01 CPU TEST		CT	ADRS	INSTRUCTION	PAGE 27
		OPCODE	OPERAND				
1965		H			1 08025	*	
1966	* SUB-RTN 19.44		CHECK MRCG				
1967	NQ	MLCWS	ATTCH,101		12 08026	0 09099 00101 7	
1968		MLCWS	NWM07,102		12 08038	0 09009 00102 7	
1969		MLCWS	ALL8IT,1C3		12 08050	D 09071 00103 7	
1970		MRCG	102,101		12 08062	0 00102 00101 \$	
1971		C	NWM07,101		11 08074	C 09009 00101	
1972		8E	NR		7 08085	J 08093 \$	
1973	H				1 08092	*	
1974	* SUB-RTN 19.45		CHECK MRWG				
1975	NR	MLCWS	DELTA,101		12 08093	D 09077 00101 7	
1976		MLCWS	NWM16,102		12 08105	0 09018 00102 7	
1977		MLCWS	ALL8IT,1C3		12 08117	0 09071 00103 7	
1978		MRWG	102,101		12 08129	D 00102 00101 *	
1979		8H	*E13,101		12 08141	V 08165 00101 1	
1980		8CE	NS,101,D		12 08153	8 08166 00101 D	
1981	H				1 08165	*	
1982	* SUB-RTN 19.46		CHECK MRNMG				
1983	NS	MLCWS	EXCLAM,101		12 08166	0 09101 00101 7	
1984		MLCWS	NWM21,102		12 08178	D 09023 00102 7	
1985		MLCWS	ALL8IT,103		12 08190	D 09071 00103 7	
1986		MRNMG	102,101		12 08202	D 00102 00101 8	
1987		8W	*E13,101		12 08214	V 08238 00101 1	
1988		8CE	NT,101,N		12 08226	B 08239 00101 N	
1989	H				1 08238	*	
1990	* SUB-RTN 19.47		CHECK MRZWG				
1991	NT	MLCWS	NWM63,101		12 08239	0 09064 00101 7	
1992		MLCWS	BLANK,102		12 08251	0 09066 00102 7	
1993		MLCWS	ALL8IT,103		12 08263	D 09071 00103 7	
1994		MRZWG	102,101		12 08275	D 00102 00101 ;	
1995		C	NWM15,101		11 08287	C 09017 00101	
1996		8E	NU		7 08298	J 08306 \$	
1997	H				1 08305	*	
1998	* SUP-RTN 19.48		CHECK MRCWG				
1999	NU	MLCWS	NWM48,101		12 08306	D 09049 00101 7	

PGLIN	LABEL	OPCODE	OPERAND	INSTRUCTION
2000		MLCWS	TPWARK,102	12 08318 D 09090 00102 7
2001		MLCWS	ALLBIT,103	12 08330 D 09071 00103 7
2002		MRCWG	102,101	12 08342 D 00102 00101 L
2003		C	NWM15,101	11 08354 C 09017 00101
2004		8E	NV	7 08365 J 08373 S
2005	H			1 08372 *
2006	* SUB-RTN 19.49	CHECK SCNL FOR MOVE NO DATA, PROPER ADDR REG STEP		
2007	NW	MLCWS	JAY,102	12 08373 D 09102 00102 7
2008		MLCWS	NWM30,103	12 08385 D 09031 00103 7
2009		SCNL	102,103	12 08397 D 00102 00103 6
2010		SAR	HOL0A2	7 08409 G 09181 A
2011	SBR	HOLCB2		7 08416 G 09186 B
2012	C	HOLDA2,300101a	CHECK AAR FOR PROPER STEPPING	11 08423 C 09181 09613
2013	BU	NW	SHOULD NOT BRANCH	7 08434 J 08552 /
2014	C	HOLDB2,200102a	CHECK BAR FOR PROPER STEPPING	11 08441 C 09186 09618
2015	BU	NW	SHOULD NOT BRANCH	7 08452 J 08552 /
2016	BH	NW,103	SHOULD NOT BRANCH WORD MARK	12 08459 V 08552 00103 1
2017	BCE	*E8,103,S	SHOULD BRANCH	12 08471 B 08490 00103 8
2018	B	NW		7 08483 J 08552
2019		SCNL	103,102	12 08490 D 00103 00102 6
2020	SAR	HOLDA2		7 08502 G 09181 A
2021	SBR	HOL0B2		7 08509 G 09186 B
2022	C	HOL0A2,3C0102a		11 08516 C 09181 09618
2023	BU	NW	SHOULD NOT BRANCH	7 08527 J 08552 /
2024	C	HDLCB2,200101a		11 08534 C 09186 09613
2025	BE	NX	SHOULD BRANCH & EXIT	7 08545 J 08553 S
2026	NW	H		1 08552 *
2027	* SUB-RTN 19.50	CHECK MLN		
2028	NX	MLCWS	NWM63,WORK6	12 08553 D 09064 09176 7
2029		MLN	BLANK,WORK6	12 08565 D 09066 09176 A
2030		BW	*E13,WORK6	12 08577 V 08601 09176 1
2031	BCE	NY,WORK6,E	SHOULD BRANCH	12 08589 B D8602 09176 E
2032	H			1 08601 *
2033	* SUB-RTN 19.51	CHECK MLZ		
2034	NY	MLCWS	NWM51,WORK6	12 08602 D 09052 09176 7

PGLIN	LABEL	CPU TEST OPCODE	OPERAND	CC01	CPU TEST OPCODE	OPERAND
2035		MLZ	ATSIGN,WORK6			
2036		BW	*E13,WORK6	SHOULD NOT BRANCH		
2037		BCE	NZ,WCRK6,3	SHOULD BRANCH		
2038		H				
2039	*	SUB-RTN 19.52	CHECK MLC			
2040	NZ	MLCWS	NWM31,WORK6			
2041		MLC	DASH,WORK6			
2042		BW	*E13,WORK6	SHOULD NOT BRANCH		
2043		BCE	PA,WORK6,-	SHOULD BRANCH		
2044		H				
2045	*	SUB-RTN 19.53	CHECK MLW			
2046	PA	MLCWS	NWM09,WORK6			
2047		MLW	EFF,WORK6			
2048		C	NWM09,WORK6			
2049		BE	P8	SHOULD BRANCH		
2050		H				
2051	*	SUB-RTN 19.54	CHECK MLNW			
2052	P8	MLCWS	ALLBIT,WORK6			
2053		MLNW	NWM00,WORK6			
2054		BW	*E13,WORK6	SHOULD NOT BRANCH		
2055		BCE	PC,WORK6,G	SHOULD BRANCH		
2056		H				
2057	*	SUB-RTN 19.55	CHECK MLZW			
2058	PC	MLCWS	PERIOD,WORK6			
2059		MLZW	NWM04,WORK6			
2060		BW	*E13,WORK6	SHOULD NOT BRANCH		
2061		BCE	PO,WORK6,W			
2062		H				
2063	*	SUB-RTN 19.56	CHECK MLCW			
2064	PO	MLCWS	DELTA,WORK6			
2065		MLCW	NWM16,WORK6			
2066		BW	*E13,WORK6,S	SHOULD NOT BRANCH		
2067		BCE	*E2,WORK6,B			
2068		H				
2069	WCP	PASS				

CPU TEST
OPCODE OPERAND

PGLIN LABEL

PGLIN	LABEL	CC01	CPU TEST	CC01	INSTRUCTION
		OPCODE	OPERAND	ADDR	
2070		BCB1	*-16	7	08900 R 08890 2
2071		8A1	*61	7	08907 R 08914 6
2072			QV	7	08914 J 08935
2073	PASS	DCW	@CC01 COMPLETE@.G	13	08921
2074	CV	MRCWG	R1CE1.333	12	08935 D 08967 00333 L
2075		MLCS	332.339	12	08947 D 00332 00339 3
2076		8	322	7	08959 J 00322
2077	RTC	8CB1	322	7	08966 R 00322 2
2078		8A1	346	7	08973 R 00346 M
2079		8	1972	7	08980 J 01972
2080		DCW	@Ma	1	08987
2081	*			6	08988 B 03618
2082	RESET	CW	JF61	7	08994 J 02000
2083		8	START	1	09001 *
2084			H		
2085	*				
2086	*				
2087	*				
2088	*				
2089	NWM00	DC	32	1	09002
2090	NWM01		016	1	09003
2091	NWM02		024	1	09004
2092	NWM03		036	1	09005
2093	NWM04		046	1	09006
2094	NWM05		056	1	09007
2095	NWM06		066	1	09008
2096	NWM07		076	1	09009
2097	NWM08		086	1	09010
2098	NWM09		096	1	09011
2099	NWM10		0A6	1	09012
2100	NWM11		0#6	1	09013
2101	NWM12		0B6	1	09014
2102	NWM13		0C6	1	09015
2103	NWM14		0D6	1	09016
2104	NWM15		0E6	1	09017

DEFINE PRECEDING BRANCH LENGTH

CONSTANTS AND WORK AREAS

PGLIN	LABEL	CPU TEST	OPCODE	OPERAND	CT	ADDRS	INSTRUCTION
2105	NWM16	S	0B6		1	09018	
2106	NWM17	0/0	0/0		1	09019	
2107	NWM18	0S6	0S6		1	09020	
2108	NWM19	0T6	0T6		1	09021	
2109	NWM20	0U6	0U6		1	09022	
2110	NWM21	0V6	0V6		1	09023	
2111	NWM22	0W6	0W6		1	09024	
2112	NWM23	0X6	0X6		1	09025	
2113	NWM24	0Y6	0Y6		1	09026	
2114	NWM25	0Z6	0Z6		1	09027	
2115	NWM27	0/0	0/0		1	09028	
2116	NWM28	0%6	0%6		1	09029	
2117	NWM29	0S6	0S6		1	09030	
2118	NWM30	0B6	0S6		1	09031	
2119	NWM31	0H6	0H6		1	09032	
2120	NWM32	0-6	0-6		1	09033	
2121	NWM33	0J6	0J6		1	09034	
2122	NWM34	0K6	0K6		1	09035	
2123	NWM35	0L6	0L6		1	09036	
2124	NWM36	0M6	0M6		1	09037	
2125	NWM37	0N6	0N6		1	09038	
2126	NWM38	0O6	0O6		1	09039	
2127	NWM39	0P6	0P6		1	09040	
2128	NWM4C	0Q6	0Q6		1	09041	
2129	NWM41	0R6	0R6		1	09042	
2130	NWM42	0-6	0-6		1	09043	
2131	NWM43	0S6	0S6		1	09044	
2132	NWM44	0T6	0T6		1	09045	
2133	NWM45	0B6	0B6		1	09046	
2134	NWM46	0A6	0A6		1	09047	
2135	NWM47	0D6	0D6		1	09048	
2136	NWM48	0E6	0E6		1	09049	
2137	NWM49	0A6	0A6		1	09050	
2138	NWM50	0B6	0B6		1	09051	
2139	NWM51	0C6	0C6		1	09052	
2140	NWM52	0D6	0D6		1	09053	

PGLIN	LABEL	CC01	CPU TEST	CC01	ADDRS	INSTRUCTION
2141	NWW53		0E6		1	09054
2142	NWW54		0F6		1	09055
2143	NWW55		0G6		1	09056
2144	NWW56		0H6		1	09057
2145	NWW57		0I6		1	09058
2146	NWW58		0J6		1	09059
2147	NWW59		0K6		1	09060
2148	NWW60		0L6		1	09061
2149	NWW61		0M6		1	09062
2150	NWW62		0T6		1	09063
2151	NWW63		0G6		1	09064
2152	NWW66		0H6		1	09065
2153	*					
2154	TABLE		DCW	0/0	1	09066
2155	PERIOD		0/0		1	09067
2156	LOZNGE		0/0		1	09068
2157	LBRAKT		0/0		1	09069
2158	LESS		0/0		1	09070
2159	ALLBIT		0/0		1	09071
2160	AMPSND		0/0		1	09072
2161			0/0		1	09073
2162	SPLAT		0/0		1	09074
2163	RBRAKT		0/0		1	09075
2164			0/0		1	09076
2165	CELTA		0/0		1	09077
2166	CASH		0/0		1	09078
2167			0/0		1	09079
2168	COPMA		0/0		1	09080
2169	PERCNT		0/0		1	09081
2170	WDSEP	DC	0/0		1	09082
2171	BKSLSH	DCW	0/0		1	09083
2172	SEGMRK		0/0		1	09084
2173	SUBLNK		0/0		1	09085
2174	POUND		0/0		1	09086
2175	ATSIGN		0/0		1	09087

PG LIN	LABEL	CC01 OPCODE	CPU TEST OPTRAND	CC01 OPCODE	CPU TEST OPTRAND	CC01 INSTRUCTION	PAGE 33
2176	CCLOCK	•	•	•	•	•	1 09088
2177	GREATR	•	•	•	•	•	1 09089
2178	TPMARK	•	•	•	•	•	1 09090
2179	QUESTIN	•	•	•	•	•	1 09091
2180	AYE	•	•	•	•	•	1 09092
2181	EEE	•	•	•	•	•	1 09093
2182	SEE	•	•	•	•	•	1 09094
2183	CEE	•	•	•	•	•	1 09095
2184	EEE	•	•	•	•	•	1 09096
2185	EFF	•	•	•	•	•	1 09097
2186	CEE	•	•	•	•	•	1 09098
2187	ATTCH	•	•	•	•	•	1 09099
2188	EYE	•	•	•	•	•	1 09100
2189	EXCLAM	•	•	•	•	•	1 09101
2190	JAY	•	•	•	•	•	1 09102
2191		•	•	•	•	•	1 09103
2192	ELL	•	•	•	•	•	1 09104
2193	EMM	•	•	•	•	•	1 09105
2194		•	•	•	•	•	1 09106
2195	CH	•	•	•	•	•	1 09107
2196	PEA	•	•	•	•	•	1 09108
2197	QUEUE	•	•	•	•	•	1 09109
2198	ARE	•	•	•	•	•	1 09110
2199	RCDMRK	•	•	•	•	•	1 09111
2200	ESS	•	•	•	•	•	1 09112
2201	TEA	•	•	•	•	•	1 09113
2202		•	•	•	•	•	1 09114
2203	VEE	•	•	•	•	•	1 09115
2204	CBLYCU	•	•	•	•	•	1 09116
2205	EKS	•	•	•	•	•	1 09117
2206	WYE	•	•	•	•	•	1 09118
2207	ZEE	•	•	•	•	•	1 09119
2208	NAUGHT	•	•	•	•	•	1 09120
2209	CNE	•	•	•	•	•	1 09121
2210	TWC	•	•	•	•	•	1 09122
2211	THREE	•	•	•	•	•	1 09123

PGIN	LABEL	CC01	CPU TEST	CT	ADDRS	CC01
		OPCODE	OPERAND			INSTRUCTION
2212	FOUR		04a		1	09124
2213	FIVE		05a		1	09125
2214	SIX		06a		1	09126
2215	SEVEN		07a		1	09127
2216	EIGHT		08a		1	09128
2217	NINE		09a		1	09129
2218	*		T		1	09130
2219	K01	DC	aMa		1	09131
2220		DCW	aNa		2	09132
2221	K02		aE+a		1	09134
2222	K03	DC	aBa		1	09135
2223		DCW	aNa		2	09136
2224	K04		aE+a		2	09139
2225	K05		aPha		1	09140
2226	K06	DC	a a		1	09141
2227		DCW	a+a		2	09143
2228	K07		aINa		1	09144
2229	K08	DC	a6a		1	09145
2230		DCW	a+a		2	09147
2231	K09		aMNa		1	09148
2232	K10	DC	a-a		1	09149
2233		DCW	a+a		2	09151
2234	K11		aPha		1	09152
2235	K12	DC	aYa		1	09153
2236		DCW	a+a		1	09154
2237	K13	DC	aMa		1	09155
2238		DCW	aNa		2	09156
2239	K14		a+a			
2240	*					
2241	WORK1	DCW	a a		1	09158
2242	WORK2		a a		1	09159
2243	WORK3		a a		2	09161
2244	WORK4		a		10	09171
2245	WORK5		aE S-a		4	09175
2246	WORK6		a a		1	09176

		OTHER CONSTANTS AND WORK AREAS	
2247	*		
2248	*		
2249	*		
2250	*		
2251	HOLDA	DCW	0 0
2252	HOLDE		0 0
2253	PCC	LOC100	LOOP COUNT COUNTER
2254	PCCWK		LOOP COUNT WORK
2255	P1		
2256	P2		
2257	TACHLD		0
2258	SPEC11	LLC	0
2259	SPEC12	00.0ATKA	
2260	SPEC13	0S.0WBS	
2261	SPEC14	0B.0SSKA	
2262	ALPHA	0B.0GT	
2263	ALFADD	0A.0THA	
2264	BETADD	0R.0D	
2265	FIVE9S	0-1.0BLA	
2266	ADDR1	01123	
2267	ADDR1	ALPHA-2	
2268	ADDR2	WORK3-2	
2269	ADDR2	FIELD1-3	
2270	FIELD1	FIELD2-3	
2271	FIELD2	FIELD3-3	
2272	FIELD3	FIELD4-3	
2273	FIELD4	09.08GA	
2274	LIMIT	09GA	
2275	LISTRT	0.1GA	
2276	LOSTRT	0.0GA	
2277	PCNT	0 / GA	
2278	LOCNT	0 0	
2279	FIVE4S		
2280	MANYS		
2281	PRODUCT		

PGLIN	LABEL	CPU TEST	CCT	CC01	INSTRUCTION
		OPCODE	ADDRS		
2282	BIGANS	a GLLB.0.11NGFEDCHAGL;B**.RQPONMLKJ-a	33	09397	
2283	MPYTBL	a NTB.0.11NGFEDCHAGL;B**.RQPONMLKJ-a	33	09398	
2284		a SEW,SWSS4,2YXhVUTS/BMT.3#0987654321 a	32	09462	
2285	*			25	09487
2286		DCW a-*0E6*0E-*0E-*0E-*0E-*0E*a		25	09512
2287		DC a+CE-00E-*EE-*0E-*0E0*0E-*0E		25	09537
2288	TRASH	a 0E-*E-*00-*0E6*0E-*0E-*0E			
2289	*				
2290	LOADER	ECU 40C			
2291	TAC0	ECU 10C0			
2292	TAC1	ECU 10C1			
2293	TAD2	ECU 10C2			
2294	TAD3	ECU 10C3			
2295	TAD4	ECU 10C4			
2296	CPU	ECU 1256			
2297	MEMSIZ	ECU 1257			
2298	TYPE	ECU 18C0			
2299	TYPCK	ECU 1845			
2300	AA	ECU 1931			
2301	BLANK	ECU TABLE			
2302	CBIT	ECU NW#00			
2303	MINUS7	ECU PEA			
2304	MINUS8	ECU QUEUE			
2305	MINUS0	ECU EXCLAM			
2306	CIVSCR	ECU WORK7			
2307	CIVOND	ECU WORK8			
2308	QUOREM	ECU P1			
2309	QUOTNT	ECU WORK10			
2310	XRO	ECU 24			
2311	TPMK	ECU NW#15			
2312	QUOT	ECU NW#31			
2313	DELT	ECU NW#47			
2314	GPMK	ECU NW#63			
2315	GMWM	ECU ALLBIT			
2316	HOLDA1	ECU MOLDA			
2317	HOLDA2	ECU MOLDA			

CC01 CPU TEST
OPCODE OPERAND
CT ADDRS INSTRUCTION

PLIN	LABEL	CC01	CPU TEST
2318	HOLDA3	ECU	HOLDA
2319	HOLDA4	ECU	HOLDA
2320	HOLDB1	ECU	HOLDB
2321	HOLDB2	ECU	HOLDB
2322	HOLDB3	ECU	HOLDB
2323	HOLDB4	ECU	HOLDB
2324	L1ORG *		
2324		£54321	
2324		£9876	
2324		£123	
2324		£45679	
2324		-45679	
2324		-54321	
2324		-1	
2324	991YA		
2324		60	
2324		67	
2324		68	
2324		61	
2324		JD	
2324		JC	
2324		RESET	
2324		KFC2	
2324		POUND	
2324		KFC7	
2324		KFC6	
2324		00C101A	
2324		00C102A	
2325	END	2000	

END OF ASSEMBLY

J02000

